

Generated Document

PATENT ABSTRACTS OF JAPAN

(21) Application number: 05210327

(51) Intl. Cl.: H01L 21/02

(22) Application date: 25.08.93

(30) Priority:

(43) Date of application publication:

10.03.95

(84) Designated contracting states:

(71) Applicant: SONY CORP

(72) Inventor: SHIBATA YOSHIAKI HAYAFUJI TAKANORI

(74) Representative:

(54) WAFER, IDENTIFICATION INFORMATION READING METHOD, METHOD AND APPARATUS FOR MANUFACTURING INTEGRATED CIRCUIT

(57) Abstract:

PURPOSE: To deal with a multikind and small quantity production by setting optimum step conditions for each one wafer.

CONSTITUTION: A step in a process managing list 12 is updated to a next step based on identification information on a wafer 16 read by an identification information reader 14 under the control of a centralized controller 11. A process condition corrector 19 retrieves a past inspection result from a process data base 21 according to a run command from the controller 11 for the next step, processes the wafer 16 by a processor M in a processing section 15 for the next step if the retrieved result is satisfied, and then inspect it by an inspecting unit T in an inspecting section 18. This inspected result is cataloged with a process data base 21 from the corrector 19.

COPYRIGHT: (C)1995,JPO

